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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,879	07/03/2003	Kenichi Kawaguchi	60188-609	4180

7590 11/29/2006

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EXAMINER	
SHAN, APRIL YING	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,879	KAWAGUCHI, KENICHI	
	Examiner	Art Unit	
	April Y. Shan	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003 and 06 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *9-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/03/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been examined.

Election/Restrictions

2. Applicant's election without traverse of electing Group I (claims 1-8), in the reply filed on 6 November 2006 is acknowledged.

3. The Applicant did not address in the response to election/restriction whether Group II (claims 9-12) are withdrawn or canceled. Thus, claims 9-12 are withdrawn from further consideration as they are non-elected claims.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. JAPAN2002-318172, filed on 31 October 2002.

Specification

5. The disclosure is objected to because of the following informalities:

For example,

On page 1, lines 6-8 of the specification, "More particularly,.....from a device at a program owner to a device at a program user." The sentence structure is grammatically incomprehensible.

Please check the specification and correct any informality the Applicant is aware of.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-8 are rejected under the second paragraph of 35 U.S.C. § 112, because the instant claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. For example, in claim 1, lines 10-16 recites "a controller for causing...." Is grammatically incomprehensible and the sentence structure is incomprehensible.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (U.S. Patent No. 6,438,694) in view of Nara (U.S. Patent No. 5,168,151)).

As per **claim 1**, Saito discloses a semiconductor integrated circuit device comprising:

a first memory (ROM 18 in fig. 3 corresponds to Applicant's first memory) for inputting and outputting data between a bus and itself (fig. 3);

a second memory (RAM 19 in fig. 3 corresponds to Applicant's second memory) for inputting and outputting data between the bus and itself (fig. 3);

a secret key holder (EEPROM 31 in fig. 3 corresponds to Applicant's secret key holder) for holding a secret key ("A crypt-key...stored in EEPROM 31" – e.g. col. 11, lines 39-40 and col. 12, lines 10-30) ;

Saito met the claim limitation of a bus port for controlling access from outside to the bus by disclosing "communication unit 23, which receives data from an external database and transfers data outside" (e.g. col. 11, lines 7-8);

a CPU (CPU 16 in fig. 3) for storing an encrypted program and a decryption program in the first memory via the bus port (col. 11, lines 36-38 and col. 12, lines 7-9),

decrypting the encrypted program by using the decryption program and the secret key, and executing the decrypted program (col. 11, lines 25-28); and

a controller for causing, the encrypted program and the decryption program are stored in the first memory (col.11, lines 36-38).

The differences between the claimed invention and Saito is that Saito does not explicitly disclose the claimed features of a controller for causing the bus port to disable access from the outside, enabling access to the first and second memories, and thereby transferring the encrypted program and the decryption program from the first memory to the second memory, disabling access to the first memory when the transfer is completed, and disabling access to the second memory when the decryption and the execution of the decrypted program are completed. However, such missing features in Saito are taught in "memory controller 40 in fig. 1 for controlling mask ROM 29 and data memory" – col. 3, lines 44-46, abstract and col. 4, lines 35-51 aforementioned Nara reference.

It would have been obvious for a person having ordinary skill in the art to incorporate such well known features as taught in the Nara reference into the Saito's device, the same field of endeavor of IC card. The motivation of doing so is "to prevent basic data from being destroyed by bugs in software or noise or an illegal program from entering a user area and to prevent the basic program from being illegally modified", as taught in col. 4, lines 37-41 of the Nara reference.

As per **claim 2**, the combined teachings of Saito and Nara disclose a semiconductor integrated circuit device as applied in claim 1. Nara met the claimed limitation by further disclosing:

a secret key access port for controlling access from the CPU to the secret key holder, wherein the secret key access port enables access to the secret key holder when the transfer is completed and disables access to the secrete key holder when the execution of the decrypted program is completed (col. 4, lines 46-51).

As per **claim 4**, the combined teachings of Saito and Nara disclose a semiconductor integrated circuit device as applied in claim 1. Nara further discloses wherein the controller controls access to the first and second memories by controlling chip select signals to the first and second memories (e.g. col. 5, lines 11-46).

As per **claim 5**, the combined teachings of Saito and Nara disclose a semiconductor integrated circuit device as applied in claim 1. Nara further discloses in col. 5, line 55- col. 6, line 33, wherein the controller includes a flag storing portion for storing first and second flags, enables access to the first and second memories when the first flag is set, disables access to the first memory when the first flag is reset and the second flag is set, and disables access to the second memory when each of the first and second flags is reset,

the bus port disables access from the outside when at least one of the first and second flags is set, and

the CPU sets the first and second flags when the encrypted program and the decryption program are inputted to the first memory, resets the first flag when the transfer is completed, and resets the second flag when the execution of the decrypted program is completed.

11. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and Nara as applied to claims 1-2 and 4-5 above, and further in view of Admitted Prior Art of the current application (Admitted).

As per **claim 3**, the combined teachings of Saito and Nara disclose a semiconductor integrated circuit device as applied in claim 1.

The differences between the claimed invention and Saito and Nara is that the latter does not explicitly disclose the claimed features wherein the CPU includes a register and erases data stored in the register if the execution of the decrypted program is completed. However, such missing features in Saito and Nara are taught in fig. 18 and page 1, line 23 – page 2, line 3 of aforementioned Admitted of the current application.

It would have been obvious for a person having ordinary skill in the art to incorporate such well known features as taught in the Admitted reference into the Saito-Nara's device, the same field of endeavor of IC card. The motivation of doing so is "to control the memory port" and "the decrypted program written in the internal RAM is

protected from being read from the memory port to the outside under the control of the control registers" as taught in page 1, line 23 and page 2, lines 2-3 of the Admitted of the current application.

As per **claim 6**, it is rejected using the same rationale as for the rejection of claim 3.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and in view of Admitted Prior Art of the current application (Admitted).

As per **claim 7**, Saito discloses a semiconductor integrated circuit device comprising:

a first memory (ROM 18 in fig. 3 corresponds to Applicant's first memory) for inputting and outputting data between a bus and itself (fig. 3);

a second memory (RAM 19 in fig. 3 corresponds to Applicant's second memory) for inputting and outputting data between the bus and itself (fig. 3);

Saito met the claim limitation of a memory port connected between the bus and the first memory to control access from the bus to the first memory by showing the connections among ROM 18, CPU BUS 32 and SYSTEM BUS 22 in fig. 4.

a secret key holder (EEPROM 31 in fig. 3 corresponds to Applicant's secret key holder) for holding a secret key ("A crypt-key... stored in EEPROM 31" – e.g. col. 11, lines 39-40 and col. 12, lines 10-30) ;

Saito met the claim limitation of a bus port for controlling access from outside to the bus by disclosing "communication unit 23, which receives data from an external database and transfers data outside" (e.g. col. 11, lines 7-8);

A CPU writing an encrypted program and a decryption program in the first memory via the bus port (col.11, lines 36-38)

The differences between the claimed invention and Saito is that the Saito does not explicitly disclose the claimed features the CPU decrypting the encrypted program by using the decryption program and the secret key, writing the decrypted program in the second memory, and executing the decrypted program a CPU having a register, and a controller including a memory initializer for erasing data in the second memory, the controller causing, when the wiring to the first memory is completed, the bus port to disable access from the outside to the bus and causing the memory port to disable the writing to the first memory and causing, when the execution of the decrypted program is completed, the CPU to erase data stored in the register and disable access to the secret key holder and causing the memory initializer to erase the data in the second memory. However, such missing features in Saito are taught on page 1, line 17- page 2, line 3 aforementioned of the Admitted of the current application..

It would have been obvious for a person having ordinary skill in the art to incorporate such well known features as taught in the Admitted reference into the Saito's device, the same field of endeavor of IC card. The motivation of doing so is to "to control the memory port" and "the decrypted program written in the internal RAM is protected from being read from the memory port to the outside under the control of the

control registers" as taught in page 1, line 23 and page 2, lines 2-3 of the Admitted of the current application.

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito and in view of Admitted Prior Art of the current application (Admitted), further in view of Nara.

As per **claim 8**, Saito discloses a semiconductor integrated circuit device comprising:

a first memory (ROM 18 in fig. 3 corresponds to Applicant's first memory) for inputting and outputting data between a bus and itself (fig. 3);

a second memory (RAM 19 in fig. 3 corresponds to Applicant's second memory) for inputting and outputting data between the bus and itself (fig. 3);

a secret key holder (EEPROM 31 in fig. 3 corresponds to Applicant's secret key holder) for holding a secret key ("A crypt-key... stored in EEPROM 31" – e.g. col. 11, lines 39-40 and col. 12, lines 15-27) ;

a decryption key holder for holding a decryption key (col. 11, lines 39-40 and col. 12, lines 10-14);

Saito met the claim limitation of a bus port for controlling access from outside to the bus by disclosing "communication unit 23, which receives data from an external database and transfers data outside" (e.g. col. 11, lines 7-8);

the CPU performing first storage for storing the encrypted decryption key and a decryption key decryption program in the first memory via the bus port (col. 11, lines 36-

38), performing first decryption for decrypting the encrypted decryption key by using the decryption key decryption program and the secret key, writing the decrypted decryption key in the decryption key holder, performing second storage for storing an encrypted program and a decryption program in the first memory, performing decryption for decrypting the encrypted program by using the decryption program and the decrypted decryption key, and executing the decrypted program (col. 11, lines 16-57 and fig. 5).

Saito did not explicitly disclose the claimed features a CPU including a register, performing first decryption for decrypting the encrypted decryption key by using the decryption key decryption program and the secret key, writing the decrypted decryption key in the decryption key holder, performing second storage for storing an encrypted program and a decryption program in the first memory, performing decryption for decrypting the encrypted program by using the decryption program and the decrypted decryption key, and executing the decrypted program. However, such missing features in Saito are taught on page 1, line 17- page 2, line 3 aforementioned of the Admitted of the current application.

It would have been obvious for a person having ordinary skill in the art to incorporate such well known features as taught in the Admitted reference into the Saito's device, the same field of endeavor of IC card. The motivation of doing so is to "to control the memory port" and "the decrypted program written in the internal RAM is protected from being read from the memory port to the outside under the control of the control registers" as taught in page 1, line 23 and page 2, lines 2-3 of the Admitted of the current application.

The combined teachings of Saito and the Admitted of the current application fail to disclose a controller for causing, when the first storage to the first memory is completed, the bus port to disable access from the outside to the bus and enabling access to the first and second memories such that the encrypted decryption key and the decryption key decryption program are transferred from the first memory to the second memory, enabling, when the transfer is completed, access to the secret key holder and disabling access to the first memory; causing, when the first decryption is completed, the CPU to erase data stored in register and disable access to the secret key holder, while disabling access to the second memory, enabling access to the first memory, and causing the bus port to enable access from the outside to the bus, causing, when the second storage to the first memory is completed, the bus port to disable access from the outside to the bus and enabling access to the second memory such that the encrypted program and the decryption program are transferred from the first memory to the second memory, enabling, when the transfer is completed, access to the decryption key holder and disabling access to the first memory, and causing, when the second decryption and the execution of the decrypted program are completed, the CPU to erase data stored in the register and disable access to the secret key holder and disabling access to the second memory. However, such missing features in Saito-Admitted are taught in "memory controller 40 in fig. 1 for controlling mask ROM 29 and data memory" – col. 3, lines 44-46, abstract and col. 4, lines 35-51 aforementioned Nara reference.

It would have been obvious for a person having ordinary skill in the art to incorporate such well known features as taught in the Nara reference into the Saito-Admitted's device, the same field of endeavor of IC card. The motivation of doing so is to "to prevent basic data from being destroyed by bugs in software or noise or an illegal program from entering a user area and to prevent the basic program from being illegally modified", as taught in col. 4, lines 37-41 of the Nara reference.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See PTO-892)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to April Y. Shan whose telephone number is (571) 270-1014. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AYS

21 November 2006
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